

**IV. Amendments to the Claims:**

This listing and version of the claims replace all prior versions, and listings, of claims in the application.

1-14. (Canceled)

15. (Currently Amended) The circuit of claim ~~13~~ 29, wherein the sensor comprises:

a voltage drop circuit coupled to the input terminal of the sensor, wherein a voltage drop occurs across the voltage drop circuit and the high state voltage is generated at the output terminal of the sensor when the input terminal of the sensor is coupled to a voltage generated by the ESD pulse; and

a device coupled to the voltage drop circuit, wherein the device is adapted to maintain the high state voltage at the output terminal, while the input terminal of the sensor is coupled to the ESD voltage pulse.

16. (Original) The circuit of claim 15, wherein the input terminal of the sensor is coupled to a voltage supply terminal.

17. (Previously Presented) The circuit of claim 15, wherein the voltage drop circuit comprises a series of diodes.

18. (Original) The circuit of claim 17, wherein the series of diodes has about 3 to about 8 diodes.

19. (Original) The circuit of claim 15, wherein the device comprises a metal-oxide-semiconductor (MOS) transistor.

20. (Original) The circuit of claim 19, wherein the MOS transistor of the device is a N-type MOS (NMOS) transistor.

21. (Original) The circuit of claim 20, wherein a gate terminal and a drain terminal of the NMOS transistor of the device are common.

22-28. (Canceled)

29. (Previously Presented) A circuit for electrostatic discharge (ESD) protection, comprising:

an ESD protection circuit having a stack of cascaded NMOS transistors configured to discharge an ESD pulse;

a sensor that senses the ESD pulse and generates a high state voltage at an output terminal of the sensor in response to the ESD pulse; and

an inverter coupled to the output terminal of the sensor and the ESD circuit, wherein the sensor applies the high state voltage to an input terminal of the inverter,

wherein an input to the stack of cascaded NMOS transistors of the ESD protection circuit is pulled down to a low state voltage by an output voltage of the inverter when the sensor senses the ESD pulse.